anticipated by Hagino, U.S. 5,304,821. Claim 23 was rejected under 35 U.S.C. §103(a) as unpatentable over Hagino in view of Clark et al, U.S. 5,178,370. Claim 25 was rejected under 35 U.S.C. §103(a) as unpatentable over Hagino.

Addressing now each of the above-noted rejections, those rejections are traversed by the present response.

It is initially noted Claim 22 has been amended by the present response to clarify a structure recited therein. More specifically, Claim 22 now clarifies the position of the third semiconductor layer by reciting "said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer and is in direct contact with said second semiconductor layer". According to that claimed structure, and with reference to Figure 3 in the present specification as one non-limiting example, the semiconductor device recited in Claim 22 includes a second semiconductor layer 42, a third semiconductor layer 43, and a fourth semiconductor layer 44. The fourth semiconductor layer 44 is provided on a surface of the third semiconductor layer 43. The third semiconductor layer 43 is interposed between the second semiconductor layer 42 and is in direct contact with the second semiconductor layer 42. That subject matter clearly shown in Figure 3 of the present specification is neither taught nor suggested by Hagino.

It is first noted that the above-noted claim amendment is not believed to raise any issue of new matter that would preclude entry of the amendment. Specifically, the subject matter clarified in Claim 22 is also evident from a recitation of previously pending Claim 22, and specifically from the recitation that "said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer"; the present amendment is merely a clarification of the position of the third semiconductor layer

and the second semiconductor layer in relation to each other. Thus, entry of the present amendment is believed to be proper.

The basis for the outstanding rejection now cites Figure 3 of Hagino as meeting the claim limitations, and particularly notes that in Figure 3 Hagino discloses a second semiconductor layer 3, a third semiconductor layer 5b, and a fourth semiconductor layer 4a. However, the structure in Hagino does not meet the claim limitations.

Specifically, as is clear from Figure 3 in Hagino the third semiconductor layer 5b is not formed in direct contact with the second semiconductor layer 3, in contrast to the requirements in the claimed invention. More specifically, in Hagino a layer 4b is provided between the third semiconductor layer 5b and the second semiconductor layer 3. The use of that P^- layer 4b in Hagino clearly indicates that there is no "direct contact" between the second semiconductor layer 3 and third semiconductor layer 5b in Hagino, in contrast to the claimed invention.

Further, the structure of the present invention provides an advantage that a manufacturing process can be simplified since it avoids the necessity for forming another semiconductor layer between the third semiconductor layer and the second semiconductor layer.

In such ways, the invention as recited in independent Claim 22, and the claims dependent therefrom, patentably defines over the teachings in Hagino.

Moreover, no teachings in Clark et al can overcome the deficiencies in Hagino.

In such ways, the invention as recited in the pending claims patentably distinguishes over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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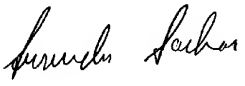

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Marked-Up Copy
Serial No: 09/421,217
Amendment Filed on:
1-3-02

IN THE CLAIMS

--22. (Twice Amended) An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof;

a second semiconductor layer of a second conductivity type provided on said first main surface of said first semiconductor layer;

a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer and is in direct contact with said second semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portion through said insulating film so that said portion forms a channel region.--